Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.025”**

**.025”**

**ANODE**

**.018 x .018”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .018” X .018”**

**Backside Potential:**

**Mask Ref: ZCA**

**APPROVED BY:DK DIE SIZE .025” X .025” DATE: 10/21/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS: .008” P/N:THZ9R1A05**

**DG 10.1.2**

#### Rev B, 7/19/02